

What is claimed is:

- 1 1. A method comprising:
2 issuing a blank check command to a memory device; and
3 reading a status bit in the memory device to verify that at least a portion of
4 the memory device is blank.

- 1 2. The method of claim 1 further comprising checking a busy bit in the
2 memory device adapted to signify that the status bit is valid.

- 1 3. The method of claim 1 wherein issuing a blank check command comprises:
2 issuing a blank check setup command; and
3 issuing a blank check confirm command.

- 1 4. The method of claim 1 further comprising specifying a block to blank check.

- 1 5. The method of claim 4 further comprising repeating the listed actions for
2 more than one block in the memory device.

- 1 6. The method of claim 4 further comprising repeating the listed actions for
2 each block in the memory device.

- 1 7. A method comprising:
2 receiving a blank check command;
3 reading a plurality of memory locations in at least one block of a memory
4 device; and
5 writing to a bit in a status register.

- 1 8. The method of claim 7 wherein receiving a blank check command
2 comprises:

3 receiving a blank check setup command; and
4 receiving a blank check confirm command.

1 9. The method of claim 7 wherein reading a plurality of memory locations
2 comprises reading each memory location in the at least one block.

1 10. The method of claim 7 further comprising:
2 setting a busy bit adapted to signify the memory device is busy; and
3 clearing the busy bit after writing to the bit in the status register.

1 11. The method of claim 7 wherein receiving a blank check command comprises
2 receiving an indication of a block to blank check.

1 12. The method of claim 11 wherein reading a plurality of memory locations
2 comprises reading memory locations in the indicated block.

1 13. A memory device comprising:
2 a FLASH memory core; and
3 a control block adapted to blank check at least a portion of the FLASH
4 memory core.

1 14. The memory device of claim 13 further comprising a status register adapted
2 to signify that the at least a portion of the FLASH memory core is blank.

1 15. The memory device of claim 13 wherein the control block comprises a state
2 machine.

1 16. The memory device of claim 13 wherein the control block comprises a
2 microcontroller.

1 17. The memory device of claim 13 further comprising an external interface
2 including a command register.

1 18. The memory device of claim 17 wherein the external interface further
2 includes a status register.

1 19. An apparatus including a medium adapted to hold machine-accessible
2 instructions that when accessed result in a machine performing:
3 issuing a blank check command to a memory device; and
4 reading a status bit in the memory device to verify that at least a portion of
5 the memory device is blank.

1 20. The apparatus of claim 19 wherein the instructions, when accessed, further
2 result in the machine performing:
3 checking a busy bit prior to reading the status bit.

1 21. The apparatus of claim 19 wherein issuing a blank check command
2 comprises:
3 issuing a blank check setup command; and
4 issuing a blank check confirm command.

1 22. The apparatus of claim 19 wherein the instructions, when accessed, further
2 result in the machine performing:
3 issuing blank check commands and reading the status bit for more than one
4 block in the memory device.

1 23. An electronic system comprising:
2 a direct conversion receiver;
3 a memory device including a FLASH memory core and a control block
4 adapted to blank check at least a portion of the memory core; and

5 a processor coupled to the direct conversion receiver and the memory
6 device.

1 24. The electronic system of claim 23 wherein the control block comprises a
2 microcontroller.

1 25. The electronic system of claim 23 wherein the memory device further
2 includes an external interface including a status register adapted to indicate whether
3 the at least a portion of the memory device is blank.

1 26. An electronic system comprising:
2 a direct conversion receiver;
3 a FLASH memory device;
4 a processor coupled to the direct conversion receiver and the FLASH
5 memory device; and
6 an article having a machine accessible medium holding instruction that when
7 accessed result in the processor issuing a blank check command to the FLASH
8 memory device and reading a status bit in the FLASH memory device.

1 27. The electronic system of claim 26 wherein issuing a blank check command
2 comprises:
3 issuing a blank check setup command; and
4 issuing a blank check confirm command.

1 28. The electronic system of claim 26 wherein the instructions, when accessed,
2 further result in the machine performing:
3 issuing blank check commands and reading the status bit for more than one
4 block in the memory device.